ET420077631US

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AUS920010302US1 PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		:	Group Art Unit:
	David W. Boerstler et al.	:	
		:	
Serial No.:		:	IBM Corporation
		:	11400 Burnet Road
Filed:	(herewith)	:	Austin, Texas 78758
		:	
Title:	ADAPTIVE PHASE LOCKED LOOP	:	Intellectual Property Law

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This Information Disclosure Statement is being submitted in connection with the above-identified application for patent. Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. § 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 C.F.R. § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists.

The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 C.F.R. § 1.98(a)(1).

A copy of each of the items identified on the attached Form PTO-1449 is supplied herewith, except for the pending patent applications, for which no copies are being submitted.

Respectfully submitted,

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In Place of FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANTS' INFORMATION DISCLOSURE STATEMENT

Serial No.:
Applicants: David W. Boerstler et al.
Filing Date: (herewith)
Group:
Atty. Docket No.: AUS920010302US1

Reference Designation

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
AAA						
ABA						
ACA						
ADA						
AEA						
AFA						
AGA						
AHA						

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
AIA						
AJA						
AKA						
ALA						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial

AMA Joonsuk Lee et al., "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 8, August 2000, pp. 1137-1145.

ANA Gyoung-Tae Roh et al., "Optimum Phase-Acquistion Technique for Charge-Pump PLL," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 44, No. 9, September 1997, pp. 729-740.

AOA Masayuki Mizuno et al., "CMOS Hot-Standby Phase-Locked Loop Using a Noise-Immune Adaptive-Gain Voltage-Controlled Oscillator," *1995 IEEE International Solid-State Circuits Conference*, pp. 268-270.

APA Rafael Fried et al., "Low-Power Digital PLL with One Cycle Frequency Lock-In Time and Large Frequency-Multiplication Factor for Advanced Pwer Management," *ICECS '96*, pp. 1166-1169.

AQA Helmuth Brugel et al., "Variable Bandwidth DPLL Bit Synchronizer with Rapid Acquistion Implemented as a Finite State Machine," *IEEE Transactions on Communications*, Vol. 42, No. 9, September 1994, pp. 2751-2759.

ARA

Examiner: Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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